

MV-VC511-7050G is a Voltage Controlled Crystal Oscillator (VCXO) . This VCXO provide low phase noise and jitter performance over a wide operating temperature range, CMOS output and comes in a hermetic ceramic 7.0x5.0mm package. This device contains an internal voltage regulator resulting in excellent power supply rejection ratio.

The device is qualified to meet the JEDEC standard for Pb-Free assembly and compliant to the RoHS directive.

#### Electrical Performance

| Parameter                             | Min       | Typ                                   | Max       | Units  |
|---------------------------------------|-----------|---------------------------------------|-----------|--------|
| <b>General</b>                        |           |                                       |           |        |
| Output Frequency                      | 10        |                                       | 250       | MHz    |
| Operating Temperature                 |           | -10/+70 to -40/+85                    |           | °C     |
| Frequency Stability                   |           |                                       |           |        |
| Stability Over Temperature            |           | ±50 to ±25                            |           | ppm    |
| Start Up Time                         |           |                                       | 5         | ms     |
| Package Size                          |           | 7.0 x 5.0 x 1.7                       |           | mm     |
| <b>Supply</b>                         |           |                                       |           |        |
| Supply Voltage (Vdd)                  |           | +2.5 to +3.3                          |           | V      |
| Supply Current                        |           | 24                                    |           | mA     |
| Current, Output Disabled              |           | 16                                    |           | mA     |
| <b>Tuning</b>                         |           |                                       |           |        |
| Absolute Pull Range                   |           | ±50                                   |           | ppm    |
| Control Voltage to reach Pull Range   |           | 1.25V±1.25V (2.5V), 1.65V±1.35V(3.3V) |           | V      |
| <b>Output</b>                         |           |                                       |           |        |
| Output Signal                         |           | CMOS                                  |           |        |
| Output Logic Level                    |           |                                       |           |        |
| Output Level - Logic High             | Vdd x 0.9 |                                       |           | V      |
| Output Level - Logic Low              |           |                                       | Vdd x 0.1 | V      |
| Output Load                           |           | 15 pF                                 |           |        |
| Output Rise and Fall Time             |           |                                       | 0.600     | ns     |
| Duty Cycle                            | 45        | 50                                    | 55        | %      |
| <b>Enable / Disable</b>               |           |                                       |           |        |
| Output Enable / Disable               |           |                                       |           |        |
| Output Enabled                        | Vdd x 0.7 |                                       |           | V      |
| Output Disabled                       |           |                                       | Vdd x 0.3 | V      |
| <b>Phase Noise &amp; Jitter</b>       |           |                                       |           |        |
| Phase Noise: (125 MHz)                |           |                                       |           |        |
| 10 Hz offset                          |           | -62                                   |           | dBc/Hz |
| 100 Hz offset                         |           | -96                                   |           | dBc/Hz |
| 1kHz offset                           |           | -111                                  |           | dBc/Hz |
| 10kHz offset                          |           | -123                                  |           | dBc/Hz |
| 100kHz offset                         |           | -127                                  |           | dBc/Hz |
| 1MHz offset                           |           | -138                                  |           | dBc/Hz |
| 10MHz offset                          |           | -155                                  |           | dBc/Hz |
| Jitter                                |           |                                       |           |        |
| RMS Jitter: (12kHz - 20MHz) - 125 MHz |           | 0.6                                   |           | ps     |

#### Notes:

- 1 Pull Range tested with Vc = 0V to 3.0V
- 2 Rise and Fall times measured from 20% to 80% of a full output swing
- 3 Power Supply pin should be filtered. e.g. 0.1µF or 0.01 µF Capacitor for optimal performance.
- 4 The Output is Enabled if the Enable/Disable is left open.

**Maximum Ratings**

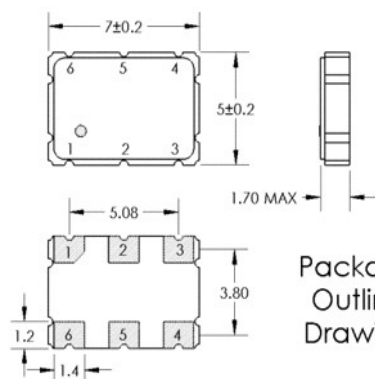
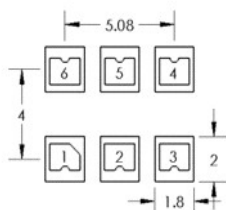
|                        |                  |
|------------------------|------------------|
| Storage Temp           | -55°C to 125°C   |
| Supply Voltage         | 4.2              |
| Enable/Disable Voltage | -0.5 to Vdd +0.5 |
| Junction Temperature   | +125 °C          |

**Maximum Ratings Notes:**

- 1 Stresses in excess of the absolute maximum ratings can permanently damage the device.
- 2 Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

**Package Information**

| Pin # | Function                     |
|-------|------------------------------|
| Pin 1 | Vc = Control Voltage or NC   |
| Pin 2 | E/D = Enable / Disable       |
| Pin 3 | GND = Ground                 |
| Pin 4 | OUT = Output                 |
| Pin 5 | C-OUT = Complimentary Output |
| Pin 6 | Vdd = Supply Voltage         |

**Pad Layout**

**Package  
Outline  
Drawing**
**Handling and Construction**

|                            |                  |
|----------------------------|------------------|
| Package Construction       | hermetic ceramic |
| Contact Pads               | Gold over Nickle |
| Moisture Sensitivity Level | MSL 1            |
| ESD, Human Body Model      | 500V             |
| ESD, Charge Device Model   | 500V             |

**Ordering Information**

**MV-VC511-7050G -    x x x C H -    xxxMxxxx**

VCXO, CMOS

7.0 x 5.0 x 1.7mm, 6 Pins

① ② ③ ④ ⑤

Frequency

① Voltage

B: 3.3 V

D: 2.5 V

② Temp Range

J: -10/+70 °C

H: -20/+70 °C

K: -40/+85 °C

③ Temp Stability

C: ±50 ppm

E: ±25 ppm

④ Absolute Pull Range ⑤ Enable

C: ±50 ppm

H: Enable High