MV-VC114-7050G

Voltage Controlled Crystal Oscillator (VCXO)
7.0 x 5.0mm - CMOS

MV-VC114-7050G is a Voltage Controlled Crystal Oscillator (VCXO) . This VCXO provide good phase noise and jitter performance over a wide operating temperature range, CMOS output and comes in a Hermetic Ceramic 7.0x5.0mm package. This device contains an internal voltage regulator resulting in excellent power supply rejection ratio.

The device is qualified to meet the JEDEC standard for Pb-Free assembly and compliant to the RoHS directive.

Electrical Performance

Parameter	Min	Typ	Max	Units
General				
Output Frequency	1		80	MHz
Operating Temperature		-10/+70 -40/+85 -40/+105 -40/+125		°C
Stability Over Temperature		±50 ±25 ±20		ppm
Start Up Time			10	ms
Package Size		7.0 x 5.0 x 1.7		mm
Supply				
Supply Voltage (Vdd)	4.75	5	5.25	V
Supply Current		5	9	mA
Current, Output Disabled		1	2	mA
Tuning				
Absolute Pull Range		±50		ppm
Control Voltage to reach Pull Range	0		Vdd + 0.5	V
Control Voltage Impedance	100			KΩ
Control Voltage Modulation BW	15			kHz
Output				
Output Signal		CMOS		
Output Logic Level				
Output Level - Logic High	Vdd-0.4			V
Output Level - Logic Low			0.4	V
Output Load		15 pF		
Output Rise and Fall Time		3.0	4.5	ns
Duty Cycle	40		60	%
Enable / Disable				
Output Enable / Disable				
Output Enabled	Vdd x 0.7			V
Output Disabled			Vdd x 0.3	V
Phase Noise & Jitter				
Phase Noise: (61.44 MHz)				
10 Hz offset		-63		dBc/Hz
100 Hz offset		-97		dBc/Hz
1kHz offset		-129		dBc/Hz
10kHz offset		-144		dBc/Hz
100kHz offset		-157		dBc/Hz
1MHz offset		-159		dBc/Hz
10MHz offset		-164		dBc/Hz
Jitter				
RMS Jitter: (12kHz - 20MHz) - 61.44 MHz		0.12		ps

Notes:

1 Pull Range tested with Vc = 0V to 3.0V
2 Rise and Fall times measured from 20% to 80% of a full output swing
3 Power Supply pin should be filtered. e.g. 0.1µF or 0.01 µF Capacitor for optimal performance.
4 The Output is Enabled if the Enable/Disable is left open.

Maximum Ratings

Storage Temp	-55°C to 125°C
Supply Voltage	-0.5V to +7.0V
Control Voltage	-0.5V to Vdd+0.5V
Enable/Disable Voltage	-0.5V to Vdd+0.5V
Junction Temperature	+150 °C

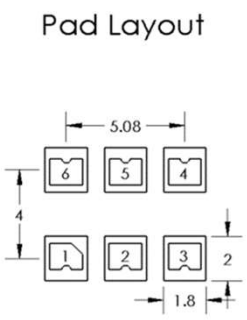
Maximum Ratings Notes:

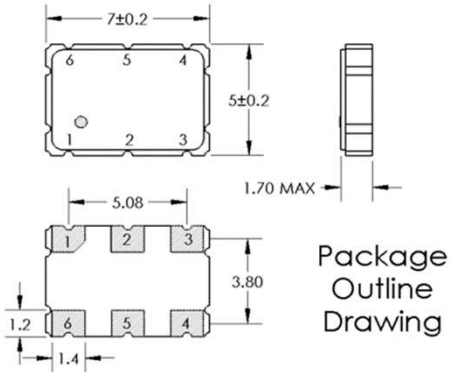
1 Stresses in excess of the absolute maximum ratings can permanently damage the device.

2 Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Package Information

Pin #	Function
Pin 1	Vc = Control Voltage or NC
Pin 2	E/D = Enable / Disable or NC
Pin 3	GND = Ground
Pin 4	OUT = Output
Pin 5	E/D = Enable / Disable
Pin 6	Vdd = Supply Voltage





Handling and Construction

Package Construction	Hermetic Ceramic
Contact Pads	Gold over Nickle
Moisture Sensitivity Level	MSL 1
ESD, Human Body Model	500V
ESD, Charge Device Model	500V

Ordering Information

MV-VC114-7050G - A x x C x - xxMxxxxx

① ② ③ ④ ⑤

VCXO, CMOS

7.0 x 5.0 x 1.7mm, 6 Pins

Frequency

① Voltage	② Temp Range	③ Temp Stability	④ Absolute Pull Range	⑤ Enable
A: 5 V	J: -10/+70 °C	C: ±50 ppm	C: ±50 ppm	2: Enable on Pin 2
	K: -40/+85 °C	E: ±25 ppm		5: Enable on Pin 5
	L: -40/+105 °C	F: ±20 ppm		